An Analog LO Harmonic Suppression Technique for SDR Receivers

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***Abstract*— A low-complexity analog technique to suppress the local oscillator (LO) harmonics in software-defined radios is presented. Accurate mathematical analyses show that an effective attenuation of the LO harmonics is achieved by modulating the transconductance of the low-noise transconductance amplifier (LNTA) with a raised-cosine signal. This modulation is performed through the bias network of a cascode device with a negligible increase in the LNTA noise figure. The proposed technique results in a notch at the third harmonic and at least 36 dB of attenuation at the fifth and the seventh harmonics. Experimental results in 130-nm CMOS and postlayout simulation results in 65-nm CMOS verify the proper functionality of the proposed technique and the accuracy of the proposed analyses.**

***Index Terms*— Blocker, filtering, interference, local oscillator (LO) harmonics, low-noise transconductance amplifier (LNTA), mixer, software-defined radios (SDRs), wideband.**

I. Introduction

SOFTWARE-DEFINED radios (SDRs) are reconfigurable systems that are able to tune to any wireless standard with variable carrier frequency, modulation type, and bandwidth. This concept is inspired by the increased demand for integrated multistandard wireless transceivers. These transceivers can support a variety of radio standards such as Global System for Mobile communications (GSM), Wi-Fi, positioning systems (GPS), Bluetooth, 3G/4G cellular, and Zigbee. The ideal SDR receiver [1] includes a wideband analog-to-digital (A/D) converter followed by a digital signal processor (DSP) that accomplishes the radio functions. However, wideband data converters require very high-power consumption [2]. Hence, in order to efficiently realize the SDR concept, mixed-signal and digital techniques can be utilized.

Reported techniques to realize mixed-signal or discrete-time (DT) SDR receivers usually include a mixing operation before A/D conversion. Mixing can be continuous or discrete in time. In [3]–[5], the receiver includes a low-noise amplifier (LNA) and a continuous-time mixer, and the sampling and conditioning of the sampled signal are realized after the downconversion at zero-IF. Several approaches use RF sampling with DT mixing. One example of this approach is proposed in [6], where the RF signal voltage is oversampled and multiplied by the oversampled local oscillator (LO) waveform for downconversion. Nowadays, direct sampling of an RF signal can be realized in highly scaled CMOS. Different RF-sampling receiver architectures are proposed in [7]–[11] working at different sampling frequencies, with different subsequent DSP techniques.

This paper presents an SDR front end with high-Q RF filtering resilient to out-of-band blockers and proposes a low-complexity analog technique for attenuation of LO harmonics. This technique can be mixed with already available DT mixing techniques to improve their harmonic rejection. This paper is structured as follows. Section II overviews the main issues of an SDR system (i.e., blockers and interference located at LO harmonics). Section III presents the proposed solution to suppress the gain at LO harmonics and the associated mathematical analyses. Experimental results in 130-nm CMOS and postlayout simulation results in 65-nm CMOS are reported in Section IV, and are compared with the theoretical equations that are derived in Section III.

II. Software-Defined Radios and Their Limitations due to Blockers and LO Harmonics

This section overviews the SDR concept and discusses its limitations due to the blockers and interferers at the LO harmonics. The traditional narrowband radios include fixed high-Q external surface acoustic wave (SAW) filters that remove out-of-band blockers, images, and interferers. Blockers can desensitize the receiver, while images and interferers can be downconverted to IF or baseband corrupting the desired signal. In a portable battery-powered handheld wideband SDR device, it is not easily possible to use SAW filters. Hence, the research focus in recent years has been noticeably focused on SAW-less wideband receivers. These receivers are software-defined for various standards, bandwidths, and frequencies. Removing any RF prefiltering causes several problems: wideband noise and large blockers that can directly leak into the receiver. Moreover, during downconversion, any unwanted signal located in LO harmonic frequencies can be easily aliased with the wanted signal at the baseband. Therefore, there are two main issues in the design of any wideband receiver front end, as depicted in Fig. 1, which must be considered: out-of-band blockers high-Q filtering to avoid gain compression, and LO harmonics rejection of the mixer to avoid aliasing.

A. Blockers

For a typical receiver, a wanted channel signal needs to be received at very low amplitude. Therefore, the receiver's

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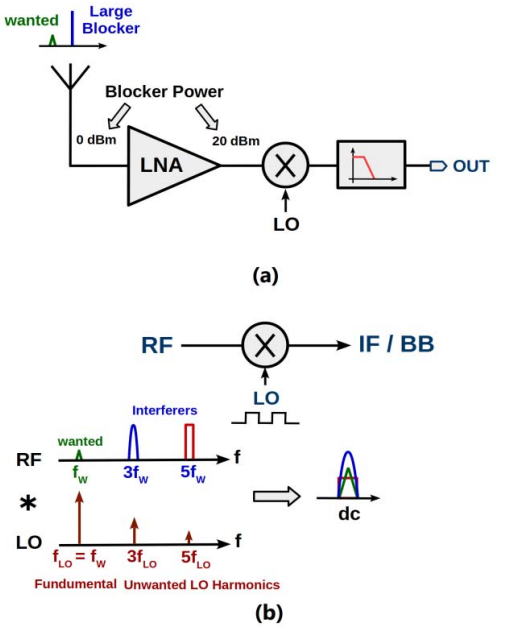

Fig. 1. Main limitations in SDR systems. (a) Blockers [12]. (b) LO harmonics.

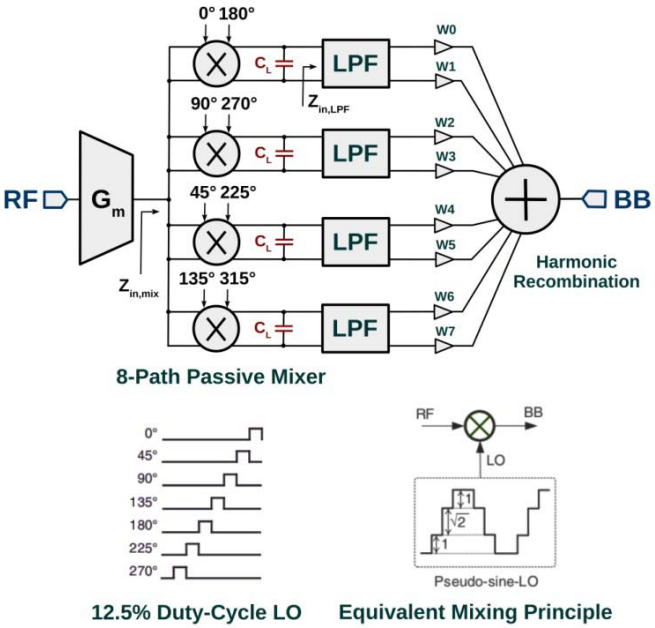

Fig. 2. General N-path architecture to achieve both blocker filtering and harmonic rejection [19].

LNA must operate at a relatively-high gain. For instance, if the gain of the LNA is equal to 20 dB, a 0-dBm out-of-band blocker results in a 632-mV blocker (assuming a 50-Ω system). This is amplified to 6.3 V and completely compresses the receiver. Hence, without external filtering, on-chip high-Q filtering is required.

Four techniques are proposed in the literature to address blockers: translational filtering [13], [14], mixer-first technique [15], [16], current-mode systems [17], and voltage-mode system with RF filtering [12], [18]. Recent work presenting a voltage-mode system with RF filtering [12], [18] includes a linear LNA that amplifies the wanted signal and rejects blockers. The high output impedance of the following switching mixer amplifies the wanted channel, while the blocker suppression is realized by designing this output impedance to be low outside of the wanted channel, where the blocker exists.

B. Interferers at LO Harmonics

Due to the nature of mixing a signal by a square wave, any undesired signal at the harmonics of the LO frequency f_{LO} also downconvert to baseband, with a conversion gain of $4/k\pi$, where k is the odd harmonic number. This conversion gain is -9.5, -14, and -17 dB at the third, fifth, and seventh harmonics, respectively. Therefore, the undesired signal at the harmonics of f_{LO} is not rejected enough by the receiver.

In order to realize a wideband receiver with harmonic suppression, different architectures have been developed. Almost all of these techniques are based on N-path filtering to realize the rejection at the harmonic frequencies. Fig. 2 shows the general architecture of a wideband receiver [19]. Although N-path techniques can deliberately reject the harmonics of f_{LO}, the nonidealities in the clock and the timing errors, including finite slopes and process–voltage–temperature-dependent mismatch errors of buffers and gates, can limit the amount of rejection. In the classical one-stage harmonic rejection mixer [20], three square-wave LOs with phases of 0°, 45°, and 90° are generated and applied to three paths that are weighted by "1: $\sqrt{2}$: 1." It can be shown that this rejects the third and fifth LO harmonics. The main drawback of this approach is that the irrational number $\sqrt{2}$ is not trivial to be accurately implemented. Moreover, the harmonic rejection ratio (HRR) is very sensitive to both gain and phase mismatches, i.e., 1° phase and 1% gain errors limit the HRR to 35 dB [19]. A two-stage technique is proposed in [17], to improve HRR, where the irrational ratio "1: $\sqrt{2}$: 1" is realized in two steps, such that it achieves a weighting ratio of 29: 41: 29 that can be realized using integer numbers. It is shown that this ratio represents only 0.03% error, corresponding to an HRR of 77 dB.

III. Proposed Technique for Harmonic Suppression

In order to improve the harmonic rejection, this paper proposes an analog technique that can be integrated with the already-proposed sampling mixer technique [12]. The proposed technique is applied to a single-path receiver architecture that results in simplified clocking and reduced power consumption, as compared to traditional N-path architectures. In this technique, the output current of the low-noise transconductance amplifier (LNTA) is modulated before the switching mixer. This technique results in a notch at the third harmonic and at least 30-dB rejection at the fifth and seventh harmonics. Fig. 3(a) shows the block diagram of a basic single-path software-defined receiver comprising an LNA with a sampling mixer, and Fig. 3(b) shows the conceptual block diagram of the proposed SDR receiver comprising an LNTA with an

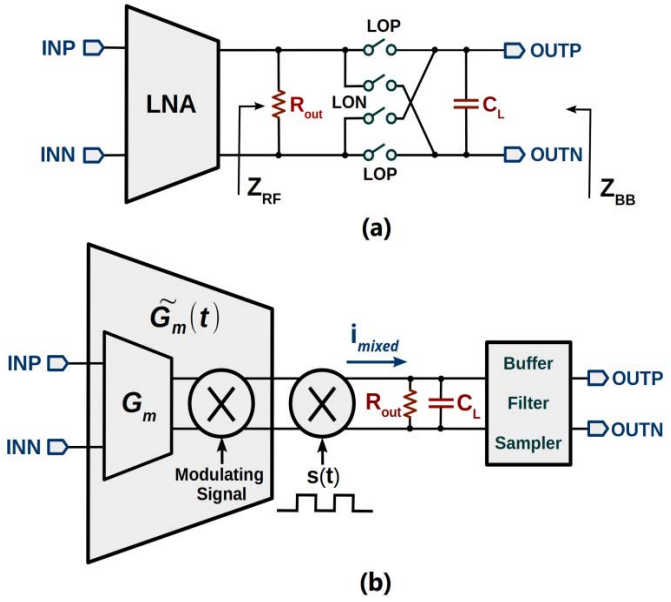

Fig. 3. (a) Block diagram of a basic software-defined receiver. (b) Conceptual block diagram of the proposed software-defined receiver with blocker resilience and improved LO harmonics rejection.

embedded time-based analog modulating element, a sampling mixer, *RC* filtering, and sampling.

A. Operation of the Proposed System

As shown in Fig. 3(b), a transconductor converts the input voltage into a current. This current is then multiplied by a modulating signal with a fundamental frequency of ω_m. The Fourier series of the resulting modulated transconductance $\tilde{G}_m(t)$ is

$$\tilde{G}_m(t) = G_0 + \sum_{k=1}^{\infty} G_k \cos(k\omega_m t) \tag{1}$$

$$G_k = \frac{2}{T_m}\int_T \tilde{G}_m(t)\cos(k\omega_m t)dt, \quad G_0 = \frac{1}{T_m}\int_T \tilde{G}_m(t)dt. \tag{2}$$

Then, the output current is multiplied by a 50% duty-cycle square-wave $s(t)$ with 1, -1 levels and the fundamental frequency of ω_c, resulting in the output mixed current of

$$\begin{aligned} i_{\text{mixed}}(t) &= V_{\text{in}}(t) \times \text{LO}(t) \\ \text{LO}(t) &= \tilde{G}_m(t) \times s(t). \end{aligned} \tag{3}$$

Here, the square-wave signal $s(t)$ has no dc and even components and can be represented as

$$s(t) = \sum_{k=1}^{\infty} \frac{2[1-(-1)^k]}{k\pi}\sin(k\omega_s t) = \sum_{k=1,3,5,\ldots} \frac{4}{k\pi}\sin(k\omega_s t). \tag{4}$$

Finally, the output mixed current flows into a baseband impedance comprising the output sampling capacitor in parallel with the output resistance of the LNA. This means that the output mixed current is low-pass filtered to remove high-frequency components

$$\begin{aligned} V_{\text{out}}(t) &= i_{\text{mixed}}(t) * h_{\text{LP}}(t) \\ &= V_{\text{in}}\left[G_0 + \sum_{k=1}^{\infty} G_k \cos(k\omega_m t)\right]\left[\sum_{k=1}^{\infty} S_k \sin(k\omega_s t)\right] \\ &\quad * h_{\text{LP}}(t) \end{aligned} \tag{5}$$

where $h_{\text{LP}}(t)$ is the impulse response of the *RC* filter, where R denotes the output resistance of transconductor and C is the sampling capacitance. Modulating G_m results in a modulation in the output resistance, and, hence, the average of value of R is used. The transfer function $H_{\text{LP}}(s)$ is given by

$$H_{\text{LP}}(s) = \frac{V_{\text{out}}(s)}{I_{\text{mixed}}(s)} = \frac{\bar{R}}{1+\bar{R}Cs}. \tag{6}$$

Here, the low-pass single-sideband (SSB) bandwidth and quality factor of the system are calculated by

$$\text{BW}_{\text{SSB,Hz}} = \frac{1}{2\pi RC} = \frac{1}{2\pi \times \bar{R} \times C} \tag{7}$$

$$Q = \frac{\omega_0}{\text{BW}_{\text{DSB}}} = \frac{2\pi f_0}{2\times\frac{1}{\bar{R}C}} = \pi \bar{R} C f_0. \tag{8}$$

B. Gain at the Fundamental and Harmonics

When the receiver is tuned for a wanted channel with a center frequency of ω_c, considering direct conversion results in $\omega_s = \omega_c$. As will be shown in the following equations, by setting the fundamental frequency of the modulating signal equals to $2\omega_c$, different harmonics of the input signal can be considerably rejected. Assuming $\omega_m = 2\omega_c$, the LO(t) can be rewritten as

$$\begin{aligned} \text{LO}(t) &= \tilde{G}_m(t) \times s(t) \\ &= \sum_{r=0}^{\infty} G_r \cos(r2\omega_c t) \sum_{k=1}^{\infty} S_k \sin(k\omega_c t) \\ &= \sum_{r=0}^{\infty}\sum_{k=1}^{\infty} \frac{1}{2} G_r S_k \{\sin(2r+k)\omega_c t + \sin(2r-k)\omega_c t\}. \end{aligned} \tag{9}$$

Considering the Fourier series for LO(t), that is

$$\text{LO}(t) = \sum_{n=1}^{\infty} L_n \sin(n\omega_s t) \tag{10}$$

the Fourier series coefficients L_n can be calculated from (9) using the convolutions of G_k and S_k as

$$L_n = \sum_{r=0}^{\infty} \frac{1}{2} G_r [S_{n+2r} + \text{sgn}(n-2r) S_{|n-2r|}]. \tag{11}$$

Here, LO(t) has a fundamental frequency of ω_m, nonzero odd harmonics, and no even harmonics. Thus, using (3), the input signals at the fundamental frequency ω_m and its odd harmonics

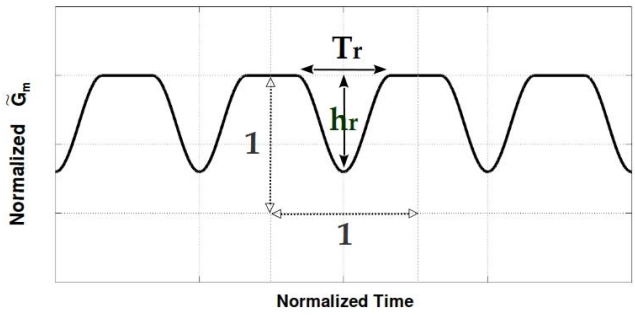

Fig. 4. Raised-cosine modulated G_m.

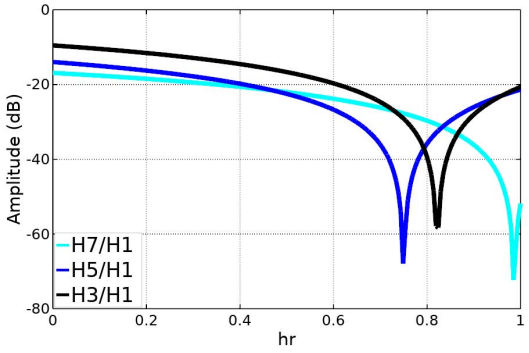

Fig. 5. Normalized amplitude setting of LO(t) Fourier coefficients for $T_r = 0.8$.

translates to the baseband. The amplitude of fundamental component is calculated as

$$L_1 = G_0 S_1 + \frac{G_1(S_3 - S_1)}{2} + \frac{G_2(S_5 - S_3)}{2} + \frac{G_3(S_5 - S_3)}{2} + \cdots \quad (12)$$

Note that with no G_m modulating signal, L_1 is $G_0 \cdot S_1$. The amplitude of the third, fifth, and seventh harmonics are equal to

$$\begin{aligned} L_3 &= \sum_{r=0}^{\infty} \frac{1}{2} G_r [S_{3+2r} + \mathrm{sgn}(3-2r) S_{|3-2r|}] \\ &= G_0 S_3 + \frac{G_1(S_5+S_1)}{2} + \frac{G_2(S_7-S_1)}{2} + \frac{G_3(S_9-S_3)}{2} + \cdots \\ L_5 &= \sum_{r=0}^{\infty} \frac{1}{2} G_r [S_{5+2r} + \mathrm{sgn}(5-2r) S_{|5-2r|}] \\ &= G_0 S_5 + \frac{G_1(S_7+S_3)}{2} + \frac{G_2(S_9+S_1)}{2} + \frac{G_3(S_{11}-S_3)}{2} + \cdots \\ L_7 &= \sum_{r=0}^{\infty} \frac{1}{2} G_r [S_{7+2r} + \mathrm{sgn}(7-2r) S_{|7-2r|}] \\ &= G_0 S_7 + \frac{G_1(S_9+S_5)}{2} + \frac{G_2(S_{11}+S_3)}{2} + \frac{G_3(S_{13}+S_1)}{2} + \cdots \end{aligned} \quad (13)$$

Using a similar method, the other coefficients can be calculated. In Section III-C, it will be discussed that with proper settings of the G_k coefficients, L_3, L_5, and L_7 can be significantly reduced, resulting in a substantial harmonic rejection.

C. Periodic Raised-Cosine Modulating Signal

To achieve harmonic rejection at the third, fifth, and seventh harmonics, the authors introduce a raised-cosine modulating signal [applied as shown in Fig. 3(b)] with the fundamental frequency of ω_m, the normalized width of T_r, and the normalized height of h_r, as depicted in Fig. 4. Although there are some other G_m modulating signals that could also be used to highly improve the rejection, not many of them can be readily realized in a circuit, The raised cosine is one of the signals that can be implemented. Different modulating signals, such as the raised cosine, triangular function, etc., are verified to effectively reject the harmonics, and based on

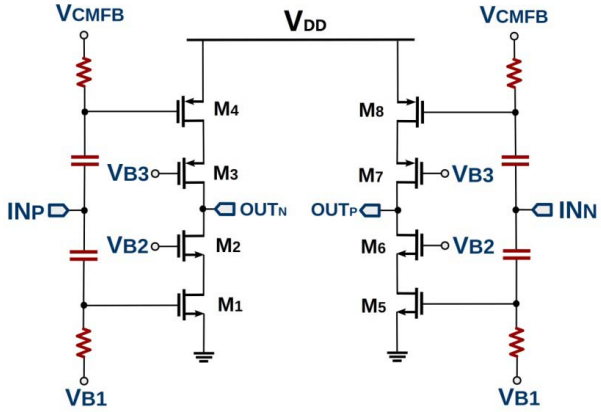

Fig. 6. Proposed LNTA utilizing a cascode transconductor.

different implementations and simulations, the raised cosine is the better solution that can be practically implemented with only a cascade device in an LNTA, as will be explained in Section III-D. For a raised-cosine modulating signal

$$\tilde{G}_m(t) = G_0 + \sum_{k=1}^{\infty} G_k \cos(k\omega_m t) \quad (14)$$

$$G_k = \frac{(h_r - 2.5)\sin(k\pi T_r)}{k\pi} + \frac{k \cdot h_r \cdot T_r^2 \sin(k\pi T_r)}{\pi(1 - k^2 T_r^2)}$$
$$k = 1/T_r, \quad k \in \mathbb{N} : G_k = -\frac{h_r}{2k_0}, \; G_0 = 1 - \frac{h_r \cdot T_r}{2}. \quad (15)$$

This G_k is then replaced in (11) to calculate the gain values at different harmonics (i.e., Fourier series coefficients L_n). Fig. 5 shows the normalized amplitude of the odd gain coefficients at $3\omega_c, 5\omega_c$, and $7\omega_c$ normalized to the fundamental gain, for $T_r \approx 0.8$ and $0 < h_r < 1$. By sweeping T_r and h_r, it is shown that for $0.75 < T_r < 0.85$ and $h_r \approx 0.8$, the normalized amplitude of the third, fifth, and seventh harmonic gains are less than -30 dB. It can be seen in Fig. 5 that there is an optimum value for h_r, where the third harmonic is completely rejected and two other harmonics are still less than -30 dB.

D. Circuit Implementation

Fig. 6 shows the cascode transconductor architecture that is utilized in this paper to realize the LNA. In standard operation, bias voltages V_{B2} and V_{B3} are dc values, which results in a

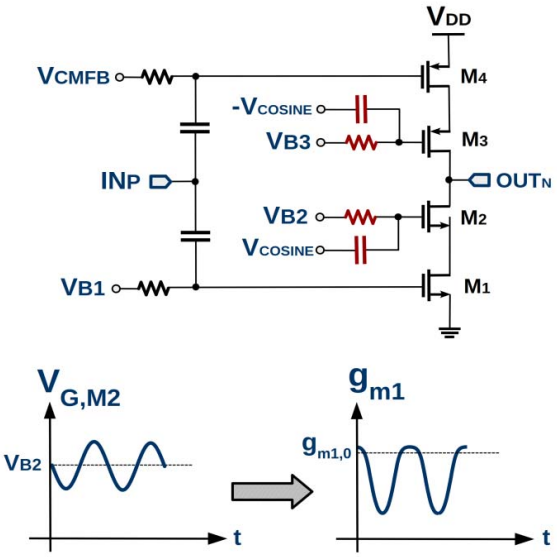

Fig. 7. Coupling the sinusoidal signal V_{COSINE} to modulate the transconductance of the G_m cell. Also shown is the signal at the gate of M_2 and the corresponding raised-cosine modulation of M1's transconductance.

constant transconductance over time and a wideband frequency range from 500 MHz to 6 GHz. Coupling a cosine signal to V_{B2} and V_{B3} can modulate the transconductance of input transistors M_1 and M_4. As shown in Fig. 7, in order to realize the raised-cosine shaping with $T_r = 0.8$, the bias voltage at the gate of M_2 is connected to V_{B2} through a resistor and to a cosine signal V_{COSINE} with a frequency of $\omega_m = 2\omega_c$ through a capacitor. Thus, V_{COSINE} changes the drain voltage of M_1 and hence, its G_m is modulated over time.

E. Foreground Tuning of the Modulation Signal Amplitude

As mentioned earlier, there is an optimum value for h_r, where the third harmonic is completely rejected and two other harmonics are still less than -30 dB.

In order to set the optimum value for h_r, a foreground technique is proposed. This technique set the amplitude of the coupled cosine signal V_{COSINE} to achieve a notch at the third harmonic. This foreground technique is an LMS loop that minimizes the output at any desired harmonic (e.g., third harmonic in this paper), as shown in Fig. 8(a). During the tuning phase, a monotone signal at the third harmonic and with a relatively large amplitude is applied at the input of the receiver. The output is at dc with a value that is proportional to the mixer gain at the third harmonic. The goal of the LMS loop is to minimize this dc amplitude and, hence, the gain at the third harmonic to improve the rejection at this frequency. This output is passed to an *RC* filter to extract its pure dc value. This dc value controls a MOS voltage-controlled resistor to tune the amplitude of V_{COSINE} that is coupled to V_{B2}, and closes the LMS loop. The simulation results of this LMS loop and the corresponding Bode plot are presented in Section IV-A.

As shown in (9), the modulated transconductance $\tilde{G}_m(t)$ and the square-wave signal $s(t)$ are based on cosine and sine elements, respectively. Since $\tilde{G}_m(t)$ is generated using

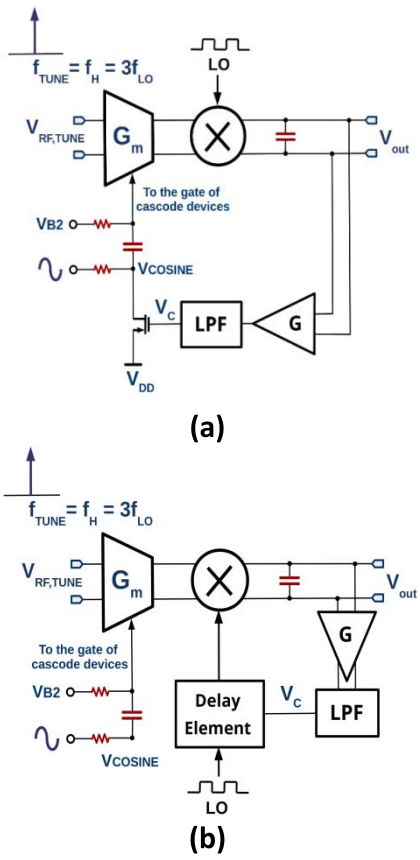

Fig. 8. Foreground tuning block. (a) Tuning the amplitude. (b) Tuning phase difference.

V_{COSINE} signal, as shown in Fig. 7, hence, V_{COSINE} and $s(t)$ must have 90° phase difference. To ensure this phase difference, a phase tuning loop is also required. This tuning loop is shown in Fig. 8(b). Here, similar to the foreground technique that sets the amplitude of V_{COSINE}, this foreground phase tuning is an LMS loop that minimizes the output at the third harmonic, by tuning the phase difference between the cosine signal and $s(t)$ through a delay-line. Note that, for simplicity, an inverter-based delay-line can be used to tune the phase of the square-wave signal $s(t)$, instead of that of the V_{COSINE} signal.

Although this tuning process is foreground and should be performed during the startup, similar to many other foreground tuning techniques, the temperature can affect the tuned coefficients. Hence, retuning is required. However, since the temperature change is a slow process, the tuning process does not need to be repeated often. Thus, although the tuning block has some area overhead, its power overhead is minimal.

F. Noise Considerations

In the following, mathematical equations to estimate the noise figure in a mixer with the proposed time-varying transconductor are presented. To verify the equations, periodic steady-state (PSS) and Pnoise simulations using the SpectreRF simulator are utilized to calculate the noise figure.

The small-signal noise factor of a differential cascode G_m cell is given by

$$\mathrm{NF} = \frac{\mathrm{SNR_{in}}}{\mathrm{SNR_{out}}} = \frac{\frac{\alpha^2(2V_s)^2}{\alpha^2 2\overline{v}_n^2}}{\frac{\alpha^2 G_m^2 V_s^2}{\alpha^2 G_m^2 \overline{v}_n^2 + \overline{i}_n^2}} \tag{16}$$

where $\alpha = Z_{\mathrm{in}}/(Z_{\mathrm{in}}+R_S)$ and $G_m = 2(g_{m1}+g_{m4})$. Moreover, $\overline{v}_n^2 = 4kTR_S$ is the average power of the source resistance thermal noise, and $\overline{i}_n^2 = 4kT\gamma G_m$ is the average power of short-circuit output current. By replacing these in (16) and simplifying it, the noise factor is obtained as

$$\mathrm{NF} = 1 + \frac{\gamma}{2\alpha^2 G_m R_S} \tag{17}$$

and the noise figure (in decibels) is equal to

$$\mathrm{NF_{dB}} = 10\log(\mathrm{NF}) = 10\log\left(1 + \frac{\gamma}{2\alpha^2 G_m R_S}\right). \tag{18}$$

In this paper, the transconductance G_m is modulated, which results in a time-varying thermal noise. An approximation for the noise figure can be written as

$$\mathrm{NF} \approx \frac{\mathrm{mean}\{\mathrm{SNR_{in}}\}}{\mathrm{mean}\{\mathrm{SNR_{out}}\}} = \frac{1}{\mathrm{mean}\left\{\frac{1}{1+\frac{\gamma}{2\alpha^2 \tilde{G}_m(t) R_S}}\right\}} \tag{19}$$

$$\mathrm{NF} \approx 1 + \frac{\gamma}{2\alpha^2 G_0 R_S} = 1 + \frac{\gamma}{2\alpha^2 R_S G_{m0}\left[1 - \frac{h_r \cdot T_r}{2}\right]} \tag{20}$$

where G_{m0} is the maximum transconductance. In order to verify this equation, it is compared with the simulated noise figure in Section IV.

IV. Simulation and Measurement Results

This section first presents the postlayout simulation results of the proposed technique to show the behavior and performance of different cells, as well as the full receiver performance in 65-nm CMOS. Finally, the experimental results of the proposed circuit implemented in 130-nm CMOS technology are presented to show the proper operation of the proposed analog LO harmonic suppression technique.

A. G_m-Cell and Modulating Technique

The proposed circuit (including the G_m cell, the switching mixer, etc.) is designed and laid out in both 130- and 65-CMOS technologies. Postlayout simulations in two different technologies are presented to show that the proposed technique is independent of the utilized technology. In standard operation of the G_m cell, bias voltages V_{B2} and V_{B3} are the dc values that result in a total transconductance G_m of 21 mS, which is relatively constant for a sideband frequency range from 500 MHz to 7 GHz. Fig. 9 shows the simulated frequency response of the G_m cell in 130-nm CMOS showing its proper operation up to 7 GHz. Moreover, the proposed circuit does not include an on-chip wideband matching network at the input, and hence, the receiver has a reduced gain. It should be noted that the harmonic rejection is the main contribution of this paper and this wideband matching network has no effect on the harmonic rejection behavior of the receiver.

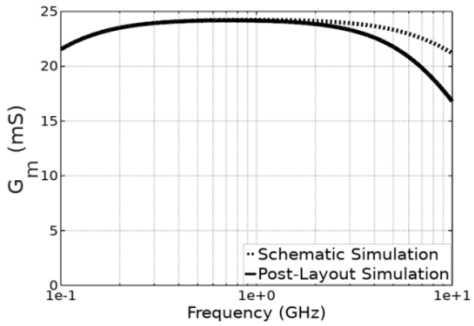

Fig. 9. Frequency response of the G_m-cell simulated in 130-nm CMOS.

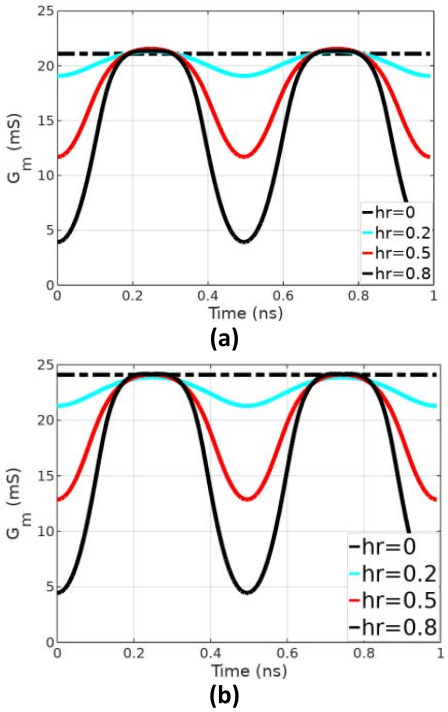

Fig. 10. Simulated G_m-cell transconductance modulated by a 2-GHz cosine for different h_r values in (a) 130- and (b) 65-nm CMOS.

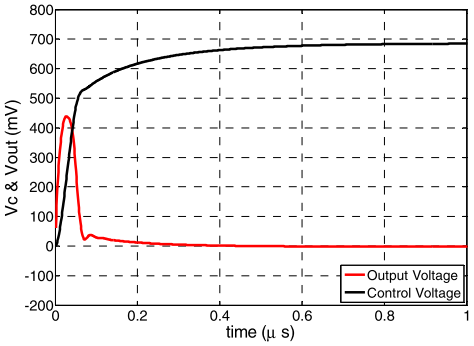

Fig. 11. Convergence of the tuning loop: output voltage V_{out} (on sampling capacitor) and control voltage V_c in Fig. 8.

In order to realize the raised-cosine modulation with $T_r = 0.8$ and different h_r, a cosine signal V_{COSINE} with a frequency of $\omega_m = 2\omega_c$ is coupled to V_{B2} and V_{B3}. Here, a V_{COSINE} with amplitude from 0 to 200 mV can modulate the G_m block over time, as shown in Fig. 10.

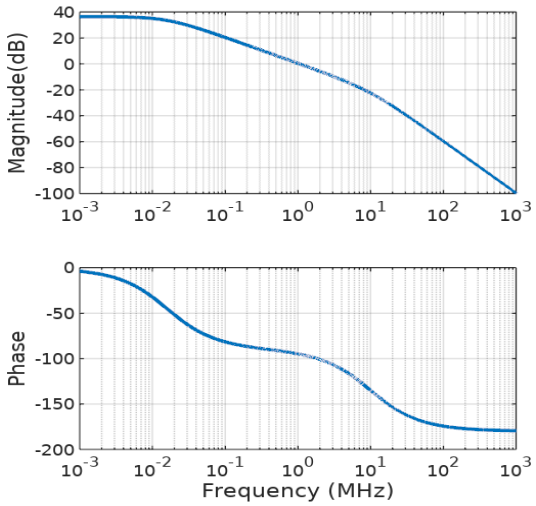

Fig. 12. Magnitude and phase response of the tuning control loop. The phase margin is 80°.

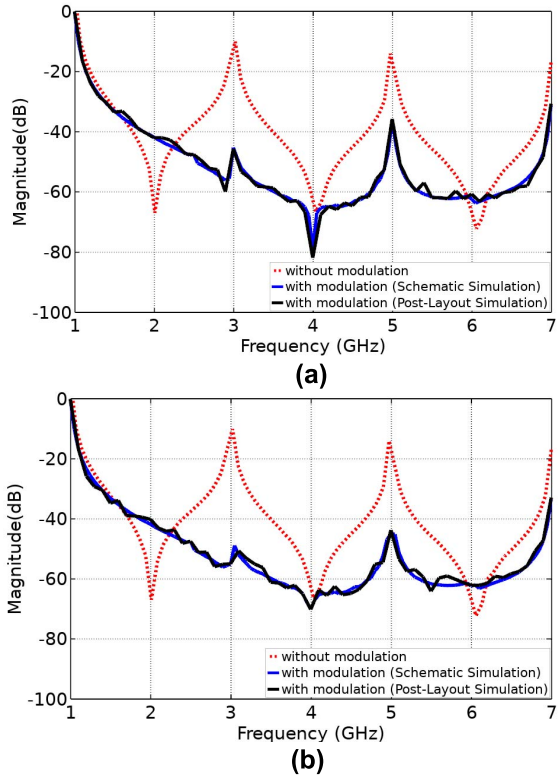

Fig. 13. Transfer function of the receiver with and without the proposed technique in (a) 130- and (b) 65-nm CMOS.

To achieve the optimum h_r value (notch in the third harmonic), the tuning block proposed in Section III is used to estimate the amplitude of V_{COSINE} and hence h_r. In the calibration phase, a 3-GHz signal with an amplitude of 100 mV is applied at the input. Here, the mixing frequency is 1 GHz. Fig. 11 shows the output voltage at the sampling capacitor and the control voltage V_c at the output of the *RC* filter during the tuning phase. As shown, the loop converges after about 0.5 μs. This value is to then be saved and used during normal operation.

Fig. 12 shows the Bode plot of the control loop, showing an 80° phase margin and a unity gain frequency of 1 MHz.

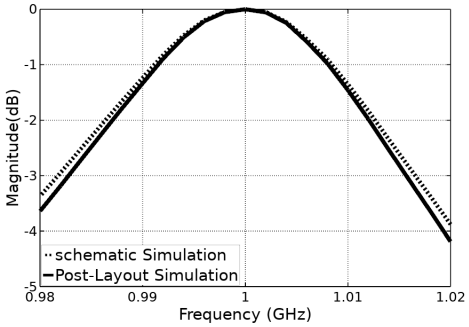

Fig. 14. Receiver frequency response around the RF frequency.

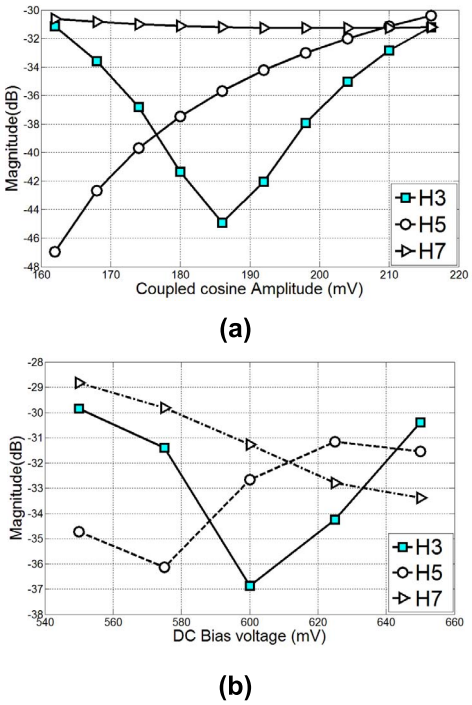

Fig. 15. Receiver gain (normalized to the fundamental gain), in 130-nm CMOS, at different harmonics versus (a) V_{B2} bias voltage and (b) amplitude of the coupled cosine signal.

Note that this Bode plot is obtained using a simplified control loop model of the tuning block, translated at the baseband. For example, the G_m cell and the sampling mixer are modeled as a "conversion gain" block at the baseband with a single pole. Moreover, the feedback path that contains an *RC* low-pass filter followed by a raised-cosine tuning mechanism is modeled as a single-pole low-pass filter with a gain factor. Hence, the receiver and the feedback path result into two single-pole systems.

B. Transfer Function and Harmonic Rejection

Fig. 13 shows the normalized transfer function of the system at an input frequency of 1 GHz for both CMOS technologies. For the optimum V_{COSINE} amplitude, there is a notch at 3 GHz and the normalized amplitude at 5 and 7 GHz are less than -30 dB, as expected. The frequency response of the system around an RF frequency of 1 GHz is simulated in 130-nm CMOS, as shown in Fig. 14, outlining the bandpass behavior of the receiver.

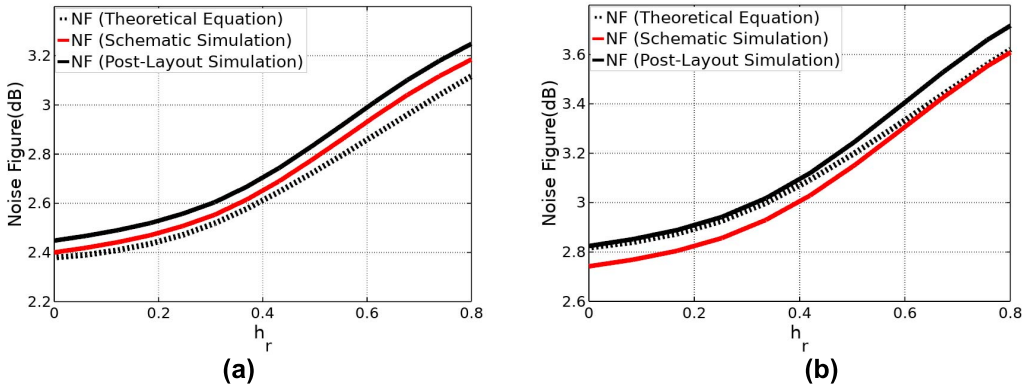

Fig. 16. Simulated noise figure at 1 GHz versus h_r using PSS and Pnoise analyses in SpectreRF and using (20) in (a) 130- and (b) 65-nm CMOS.

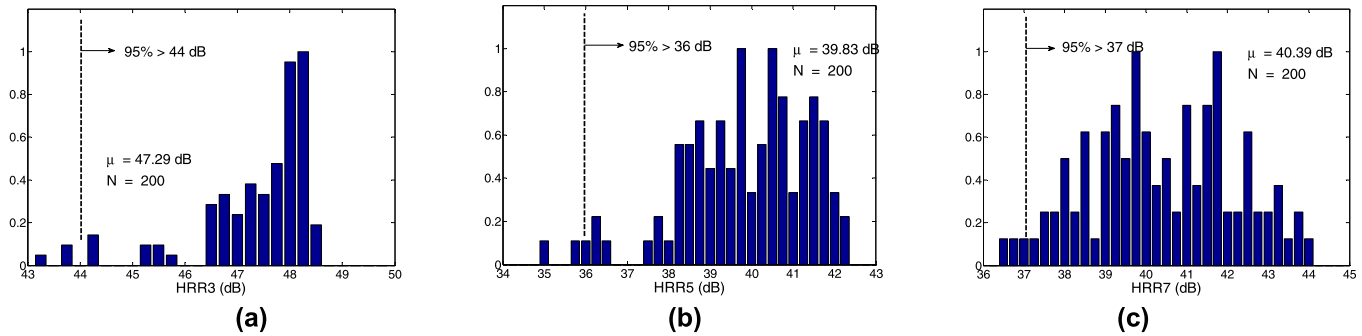

Fig. 17. Monte Carlo simulation results (normalized) of the receiver. (a) HRR3. (b) HRR5. (c) HRR7. As shown, 95% of the samples have greater than 44, 36, and 37 dB of HRR3, HRR5, and HRR7, respectively.

To characterize the sensitivity of the system to the V_{B2} bias voltage, and the amplitude of the coupled cosine signal, these parameters are varied around their nominal values. Fig. 15(a) shows the normalized magnitude of the harmonics versus the amplitude of V_{COSINE}. For a voltage interval of 160–230 mV, all of the harmonics are less than −30 dB. Here, the optimum value is 185 mV, where the third harmonic is completely rejected and the two other harmonics remain lower than −30 dB. Note that the tuning block converges to 178 mV for this amplitude. Fig. 15(b) shows the sensitivity to bias voltage V_{B2}. For V_{B2} of ±30 mV, the harmonic suppression is still better than −30 dB. Moreover, to characterize the sensitivity of the HRR to the temperature, a simulation is performed. The results show that for a 10 °C change in temperature, the depth of the third-harmonic notch is degraded by less than 2 dB.

C. Noise Figure and Power Consumption

PSS and Pnoise simulations in SpectreRF are performed on the utilized cascode G_m cell, considering the proposed modulation technique. Fig. 16 shows the noise figure plotted versus h_r as obtained from theoretical equation (20) and the simulation results.

As shown in Fig. 16, when no modulation is applied, the noise figures are 2.4 and 2.8 dB for the 130- and 65-nm designs, respectively. After applying the proposed modulation technique with $h_r = 0.8$, the noise figures are increased by only 0.7 and 0.8 dB, for the 130- and 65-nm designs, respectively. Thus, the noise performance is not significantly affected by the proposed technique. Fig. 16 also shows the accuracy of (20).

It should be noted that the modulation of the transconductance reduces the average current, resulting in reduced power consumption of the G_m cell. Here, based on the simulations, the modulation of the transconductance leads to a 30% reduction in the G_m-cell power consumption. In the simulation, the power consumption of the distribution path and circuitries required for the modulation technique are included in the total power consumption. However, the power consumption needed to generate the cosine signal is not included.

D. Montel Carlo Simulation Results

In order to fully consider the mismatches between different devices and their effect on the realized raised-cosine modulation, a Monte Carlo simulation on the full receiver is performed. This Monte Carlo simulation considers both of the mismatches between devices and different process corner models for the devices. In each Monte Carlo simulation run, the tuning block first locks to the proper value of h_r, and then the circuit operates in the normal condition and the HRR is characterized for different harmonics. Fig. 17 shows the histogram of the HRR values for the third (HRR3), fifth (HRR5), and seventh (HRR7) harmonics with a 1-GHz input signal. As shown, 95% of the samples have greater than 44, 36, and 37 dB of HRR3, HRR5, and HRR7, respectively.

E. Measurement Results

The proposed G_m cell that is accompanied by a sampling mixer to sample the downconverted output on sampling capacitors C_s was fabricated in a 130-nm CMOS technology and

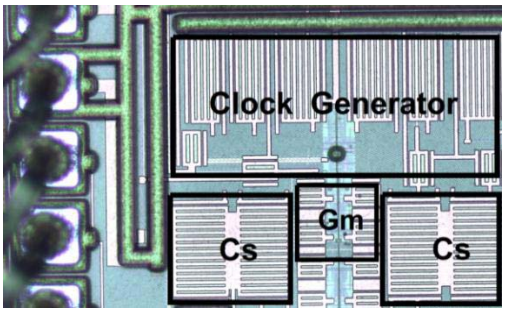

Fig. 18. Micrograph of the receiver front-end die in 130-nm CMOS. The circuit occupies a 0.25-μm^2 area on silicon.

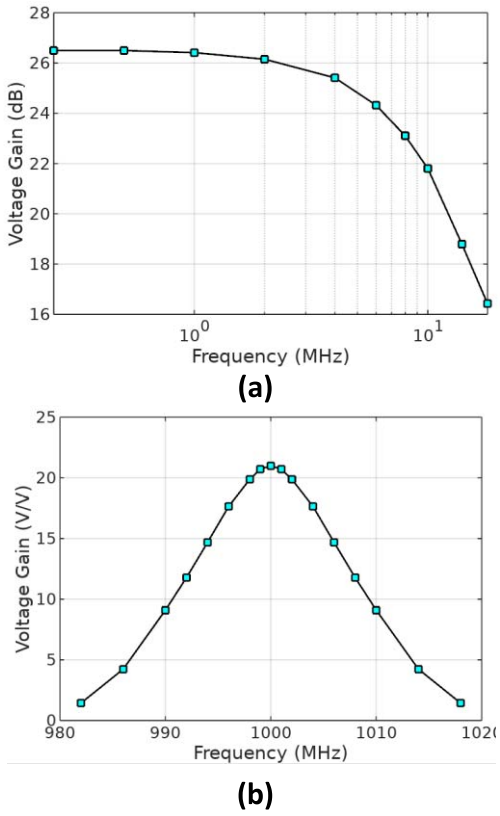

Fig. 19. Conversion gain of the receiver front end (a) at the baseband (SSB, in decibels) and (b) around RF in V/V (double-sideband), both for $f_S = 1$ GHz.

packaged in a 48-pin 7×7 mm^2 quad-flat no-leads package. The fabricated chip micrograph is shown in Fig. 18. The proposed G_m cell that precedes the sampling mixer provides the conversion voltage gain for the fundamental signal, from RF to baseband. The gain at the harmonic frequencies should be noticeably reduced due to the proposed technique. The proposed modulation is tuned to reject the third harmonic as previously discussed. Experimental results at $f_s = 1$ GHz exhibit a conversion gain of 26.5 dB for the circuit. Here, the input is swept around a 1-GHz RF, and the output is at the baseband. In Fig. 19(a), the conversion gain is plotted versus the baseband frequency (SSB), and in Fig. 19(b) it is plotted versus the input RF frequency.

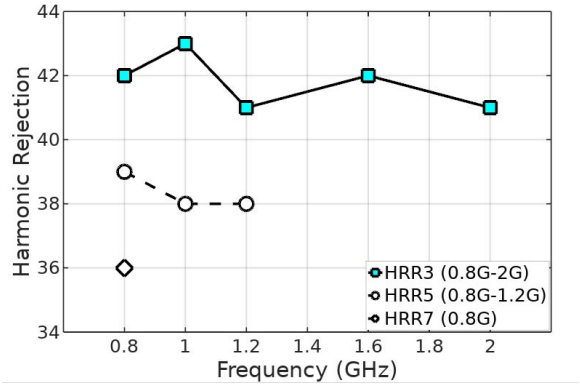

Fig. 20. Measured harmonic rejection versus input frequency, in 130-nm CMOS.

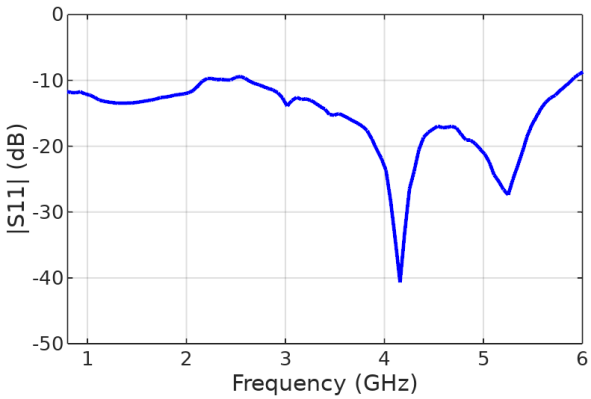

Fig. 21. Measured $|S_{11}|$ versus frequency for $f_S = 1$ GHz.

The harmonic rejection versus input frequency is measured and plotted in Fig. 20. Since the receiver operates from 0.8 to 4 GHz, to guarantee its proper operation, it is designed to reject harmonics of up to 6 GHz. Thus, harmonic rejection tests are performed for input RF frequencies of up to 2, 1.2, and 0.8 GHz, for the third, fifth, and seventh harmonics, respectively. Note that here, the calibration loop and the input matching is implemented off-chip. In the off-chip calibration loop, as shown in Fig. 8, the gain and low-pass filter blocks are implemented using an AD620 instrumentation amplifier, with a gain and bandwidth set to 5 V/V and 2.5 MHz, respectively. Moreover, although the original design has no input matching, its input matching is improved by using a large off-chip resistor from the input signal to ground in order to achieve an S_{11} below -10 dB. Starting from large values, this resistor is selected iteratively. Fig. 21 shows the measured $|S_{11}|$ versus frequency.

The phase tuning loop is also implemented off-chip and the phase of the LO signal $s(t)$ is tuned in 1° steps, so that the third harmonic rejection is maximized. Note that based on our experiment, a phase error of $\pm 2°$ does not affect the third harmonic notch depth. Hence, on-chip implementation of this calibration loop requires a delay line with 4° steps.

Table I shows the performance summary of the proposed receiver and compares it to the state of the art. As shown in Table I, the power consumption is significantly lower than

TABLE I
PERFORMANCE SUMMARY AND COMPARISON TO THE STATE OF THE ART

	This work			[16] Andrews [ISSCC'10]	[22] Murphy [JSSC'12]	[17] Ru [JSSC'09]	[3] Bagheri [JSSC'06]	[18] Chen [JSSC'14]	[21] Liempd [JSSC'14]	[23] Murphy [JSSC'15]
	Post-Layout		Measurement							
CMOS Technology (nm)	65	130	130	65	40	65	90	65	28	28
Supply Voltage (V)	1.2	1.5	1.5	1.2 / 2.5	1.3	1.2	1 / 2.5	1.2	0.9	1
Frequency (GHz)	0.8 ~ 7	0.8 ~ 7	0.8 ~ 4	0.4 ~ 6	0.08 ~ 2.7	0.4 ~ 0.9 [3]	0.8 ~ 5	0.5 ~ 3	-	0.6 ~ 3
NF (dB)	3.2 @ 1 GHz	3.3 @ 1 GHz	4 @ 1 GHz	5.5	1.5 ~ 2.5	4	5 ~ 5.5	5.5 ~ 7.8	1.8 ~ 2.4	3
In-Band IIP3 (dBm)	-3	-1	-3.5	-	-	3.5	-3.5	> -12	-	-
HRR3, HRR5 (dB)	47.2,39.8 [4] @ 1 GHz input	45,38[4] @ 1 GHz input	43, 38 @ 1 GHz input	35.4 , 42.6	42 , 45	> 60, > 64 @ 1 GHz input [5]	38, 40	50, 52 @ 1 GHz input [5]	> 70, > 75 with cal.	52, 54
HRR7 (dB)	40.3 [4] @ 1 GHz input	41 [4] @ 1 GHz input	36 @ 0.8 GHz input	-	-	-	-	-	-	-
Power Consumption (mW)	4[1]	7[1]	7[1]	37 ~ 70 [2]	35 ~ 78 [2]	60 [1]	>100 [2]	250 ~ 600	<40	38.8 ~ 70 [2]

[1] Without the frequency synthesizer and baseband processing.
[2] Without the frequency synthesizer.
[3] LO frequency range. Measurement RF bandwidth is up to 6 GHz.
[4] Average harmonic rejection, based on Monte-Carlo simulation.
[5] Extracted from figures.

the other works, while the harmonic rejection numbers are still comparable. This outlines the power consumption advantage enabled by the proposed technique.

To extend this receiver to an I/Q receiver system, two separate receivers must be used. All of the clock phases and the cosine signal of the I path must have a 90° phase shift to those in the Q path. In some techniques, the I and Q paths can share the G_m cell [12], [18]; however, here, two separate G_m cells are required since the G_m modulation signal in the Q path has a 90° phase shift with respect to that of the I path.

V. CONCLUSION

This paper presented a low-complexity analog technique to mitigate LO harmonic mixing in SDR applications. It is shown that modulating the transconductance of the LNTA with a raised-cosine signal attenuates the LO harmonic mixing gain. This transconductance modulation is implemented using the bias voltage of a cascode device. The increase in the noise figure due to the proposed technique is negligible. Moreover, the amount of suppression of the proposed technique in different LO harmonics is analytically verified. The technique was demonstrated to effectively improve the harmonic rejection with relatively low-power consumption. It was also shown to apply uniformly to two CMOS technology nodes: 65 nm (postlayout simulation) and 130 nm (measurement).

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